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Processing of Patterned Ferroelectric Capacitors

by Bernard J. Rod

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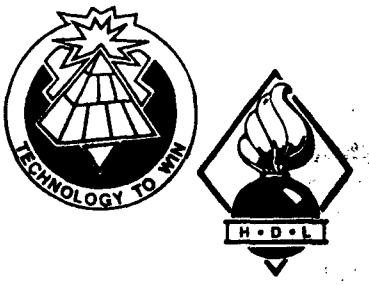

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13. ABSTRACT (Maximum 200 words)

Processing steps are described in detail for a procedure to fabricate sol-gel-derived lead-zirconate-titanate (PZT) ferroelectric thin-film capacitors in a manner compatible with processed complementary metal-oxide-semiconductor (CMOS) integrated-circuit wafers. The intended purpose of this work is to fabricate nonvolatile-element memory test structures for electrical and radiation characterization studies. A number of critical processing issues dealing with the etching of the PZT films and the deposition and definition of the top and bottom platinum electrodes were addressed and suitable solutions found during the course of this work. Using the procedures described herein, we fabricated working PZT capacitors and evaluated them electrically.

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Contents

Figures

Table

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1. Introduction

During the last few years, considerable interest has been rekindled in the application of ferroelectric materials to fabricate nonvolatile random-access memories (RAMs) that use a ferroelectric capacitor as the basic memory storage element [1–3]. Ferroelectric memories could be expected to be superior to memories based on standard technologies, not only because of their nonvolatility but also because the ferroelectric capacitor memory element itself is inherently radiation hard. In addition, because the dielectric constant of the ferroelectric material is considerably higher than that of silicon dioxide, the capacitor elements can be made much smaller than in conventional silicon-dioxide-based circuitry, and thus a significant increase in circuit component density and speed is a very real possibility. These advantages could be of considerable importance to advanced military ground and space-based electronics systems.

This report discusses a procedure developed to fabricate lead-zirconate-titanate (PZT) thin-film ferroelectric capacitors in a manner compatible with complementary metal-oxide semiconductor (CMOS) processed integrated circuits in order to produce memory element test chips; the resulting chips can be used for electrical and radiation characterization studies for the development of nonvolatile memory circuits. Figure 1 shows the basic ferroelectric capacitor structure and figure 2 shows a simplified schematic of a single memory element. The critical process steps needed to fabricate this device are the deposition and etching of the PZT films and the deposition and etching of the platinum top and bottom electrodes.

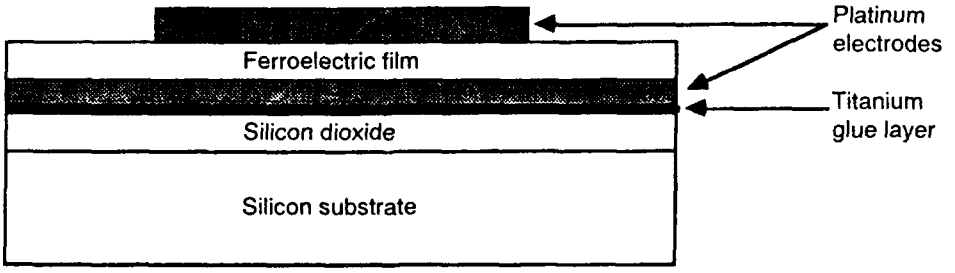


Figure 1. Ferroelectric capacitor cross section.

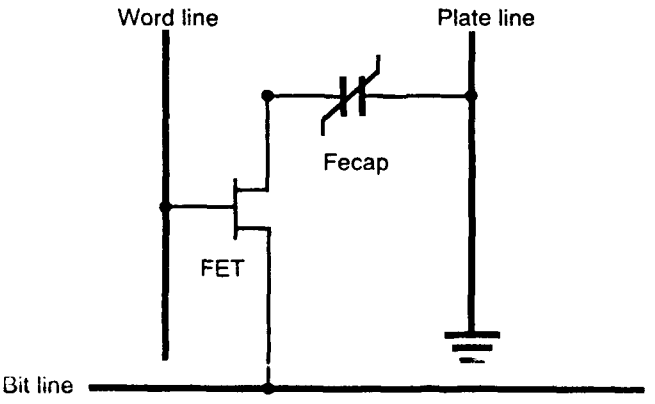


Figure 2. Memory element schematic.

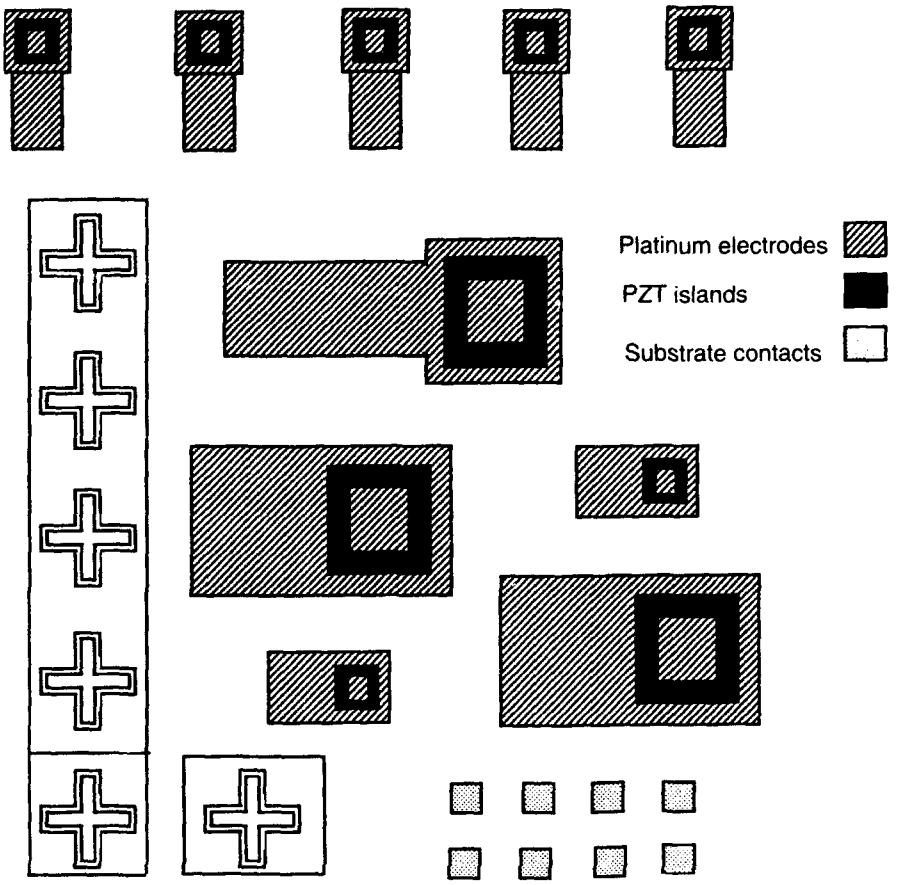
Any number of different approaches can be taken to fabricate a working ferroelectric capacitor as an independent device in itself. However, when the capacitor is to be incorporated onto a wafer with existing CMOS integrated circuitry, a number of constraints are necessarily placed on its fabrication. Some of the concerns that must be adequately addressed in producing a CMOS-compatible ferroelectric memory element are the effects of high temperatures after integrated circuit processing, exposure to potentially contaminating substances, and removal or chemical attacking of the underlying circuitry by the processing chemicals. Thus, the critical process development issue to be addressed is the compatibility of the ferroelectric capacitor process with the underlying CMOS circuitry.

All the work discussed herein is based on the processing of PZT ferroelectric films deposited by the sol-gel process [4–5]. The sol-gel and hydrolyzing solutions used during the course of this work were obtained from outside sources, but the film depositions and annealing were done in our laboratory at Harry Diamond Laboratories (HDL). The actual sol-gel deposition process itself is not considered here since this will be the subject of a separate report. Furthermore, the PZT film may be deposited in a number of different ways and, other than minor differences in the etching times due to different film thicknesses and densities, there would be no effect on the subsequent processing sequence to be discussed here.

2. Mask Set

A mask set was generated to provide devices suitable for the process development work. Two basic capacitor structures employing a 40- × 40-μm and an 80- × 80-μm square-top platinum electrode were designed for this work. In part, these sizes were designed to permit the structure to be probed directly using a standard wafer probe station. The 80- × 80-μm device should also be large enough for wire bonding using a properly adjusted ball bonder. The mask levels provide for the etching of the top and bottom electrodes and the PZT island. For this initial effort, the PZT island was designed to be considerably larger than the top electrode. This design was intentional because it was not known just how much undercutting of the PZT would occur during the etching process, and this was one of the issues to be examined in this work. In an actual device intended for a memory element in an integrated circuit, the PZT island border need only be large enough to prevent shorting between the top and bottom electrodes. Although the actual sizes of the capacitors fabricated here are larger than what would be required for an integrated circuit memory element, the basic structure is the same. Figure 3 shows a composite of the three levels used in this work.

Figure 3. Composite of mask levels.



3. Photoresist Processing

Standard photoresist procedures were used to pattern the platinum and PZT during the fabrication of the capacitors, but with some modifications to the exposure and development times as discussed below. We used KTI 820 dyed and undyed photoresists with generally very acceptable results for all the work discussed here. The resist was spun onto the wafers at 5000 rpm and then soft-baked in an air oven at 105°C for 30 min. This procedure results in a photoresist film about 1.2 μm thick. An Optometrix 8010 wafer stepper employing a multi-frequency light source and G-line filter was used to expose the photoresist. For the PZT islands, undyed resist was used with a 2.5-s exposure. For the platinum levels, the dyed resist was used, and it was found that the exposure time had to be increased to 5 s or even longer to permit adequate exposure of the resist. This additional exposure time is believed to be caused by the strong internal reflections in the resist from high reflectivity of the underlying platinum.

Following the exposure, the resist was developed in KTI 934 100-percent positive photoresist developer diluted 1:1 with deionized water. Although

the recommended development time was 30 s, we found that on occasion it was necessary to increase this to as much as 50 s to adequately develop out the patterns on the highly reflective platinum surface. We did not observe any problems with the developed images as a result of the increased development times. Increasing the exposure even more could possibly reduce the development times, but this might also lead to overexposure of the pattern. Visually, the longer development times did not adversely affect the developed patterns. After developing the photoresist, a standard hard-bake in an air oven at 140°C for 30 min was used to remove any remaining solvents from the resist and harden it. However, we found that a longer bake time of up to 40 min was desirable to additionally harden the resist before any sputter etching.

Finally, the wafers were placed in an oxygen plasma asher for 15 to 30 s at 300 W, to remove any remaining photoresist film in the areas to be etched. The removal of this film is especially important when employing wet etching procedures because even a very thin film of photoresist can prevent the intended etching action from occurring. Some patterned photoresist loss does occur during the oxygen plasma ashing process, but this loss is not significant. This plasma ashing step was usually omitted when sputter etching was employed since the sputtering would quickly remove any remaining thin photoresist film in the areas to be etched.

4. Capacitor Process Sequence

Figure 4 shows the overall processing sequence. The starting material consisted of 4-in.-diam <100> silicon wafers of varying resistivity that had been cleaned using standard wafer cleaning procedures and then thermally oxidized using either dry or wet oxidation processes to produce oxide layers several hundred to a few thousand angstroms thick. The actual oxide thickness was not considered critical to this work, and oxidations were performed in whichever furnace tube was available at the time.

Following oxidation, the wafers were placed in a Materials Research Corporation (MRC) multitarget sputtering system for the bottom electrode deposition. This deposition consists of a titanium glue layer about 300 Å thick followed immediately, and without breaking vacuum, by a platinum layer about 1700 to 3000 Å thick. Before the deposition, we pumped the sputtering system down to a pressure of 4×10^{-4} Pa. A 2-min pre-sputter against the shutter cleaned the target before we sputter-deposited the appropriate metal. Power levels of 125 and 60 W into 5-in.-diam targets were used for the titanium and platinum, respectively. These sputtering conditions resulted in deposition rates of about 50 Å/min for the titanium and 200 Å/min for the platinum.

At this point the substrates were ready for the ferroelectric film to be applied. Figure 5 shows the procedure we used to apply the PZT films in our laboratory. Film thicknesses resulting from this procedure ranged from

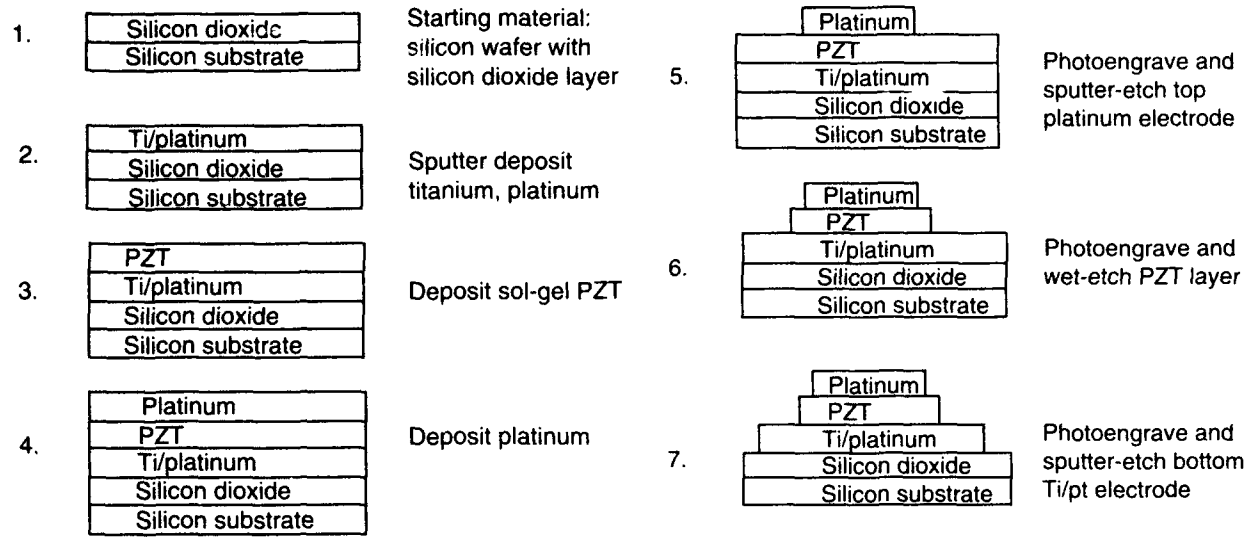
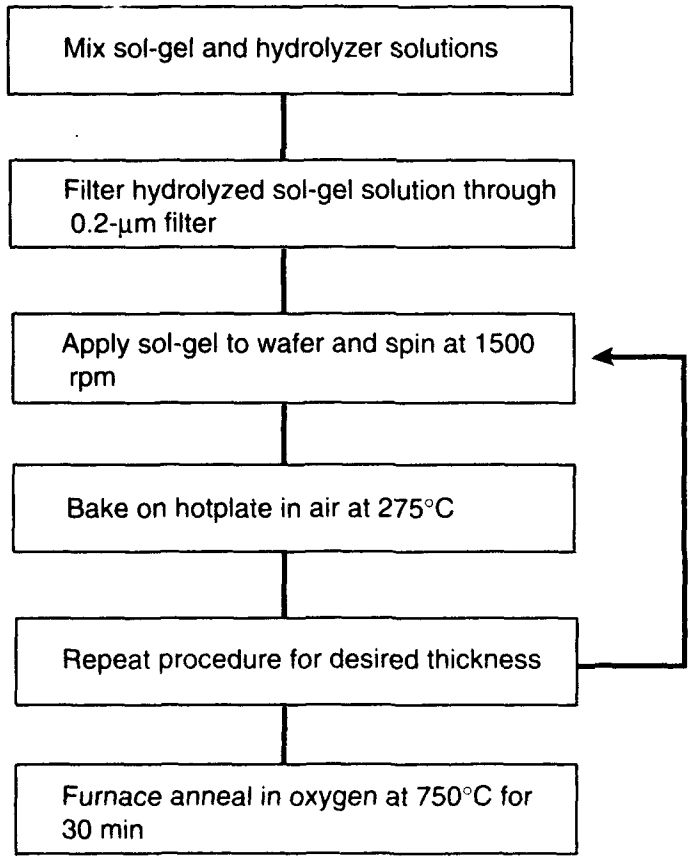


Figure 4. Processing sequence.

Figure 5. Sol-gel process.



about 2000 to 2500 Å. We used a standard diffusion furnace with an oxygen flow of 2 liters/min for the annealing step. It should be pointed out here that we did not attempt to optimize the ferroelectric film properties for our work, but rather were more concerned with the effects of the subsequent processing on the films after they were applied. At any rate, based on our previous experience with this process, we expected the ferroelectric films to have reasonably good electrical and mechanical properties.

The next step is to sputter-deposit the top platinum electrode. Since surface contamination of the PZT film before this step can seriously degrade the quality of the ferroelectric capacitor, the platinum should be deposited as soon as possible after the PZT films are applied. One technique that can be used to address the problem of potential surface contamination is to slightly sputter-etch the PZT film just before the actual platinum deposition. However, since we deposited the platinum immediately following the ferroelectric film anneal, we did not feel that it was necessary to do this for our work. The platinum sputtering conditions we used were 125 W for 6 min to give a platinum thickness of about 2 kÅ.

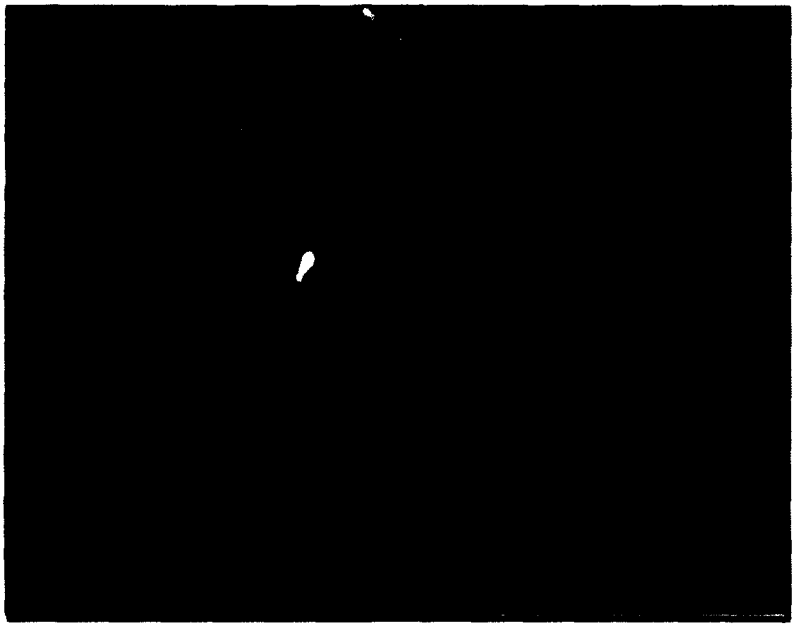
Following this platinum deposition, the top electrode was patterned and etched. To etch platinum deposited on a PZT film, some type of dry etching technique needs to be used because wet platinum etches attack the PZT film, resulting in heavy undercutting and in some cases complete pattern removal. One dry etching technique that can be used here is ion milling, which has been shown to be quite effective for this purpose. However, since an ion miller was not available to us during this work, we used a sputtering system in the etch mode to sputter-etch the platinum on the PZT. Before any actual etching was done, a number of runs were made to establish the relative sputtering etch rates of the platinum, PZT, and photoresist. Table 1 shows the etch rates for these materials at a 60-W input power. It can be observed that there is excellent etch rate selectivity between the platinum and the PZT, but that the photoresist has a relatively high sputtering rate. Nevertheless, the 1.2 μm thickness of the photoresist is more than adequate to mask the platinum electrode during the approximately 25 min required to completely etch the 2000 Å platinum layer. Figure 6 shows the etched platinum electrodes with the remaining photoresist on top. The photoresist was removed by oxygen plasma ashing for 6 min at 300 W.

At this point, the capacitors can be probed to verify proper electrical functioning. However, it is first necessary to remove a small area of PZT film to expose the bottom platinum electrode. This can be done either by mechanically abrading away the film, or by placing small drops of hydrofluoric (HF) and then 5-percent nitric acid on the film to etch it away in a suitable region such as the edge of the wafer. Figure 7 shows the hysteresis loops obtained from the 40- and 80-μm platinum electrode devices. The remanent polarization calculated from these measurements is about 25 $\mu C/cm^2$ ($2 \times Pr$).

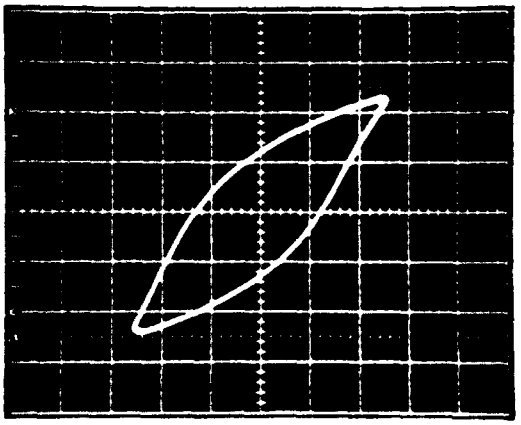
Table 1. Sputter-etch rates for process materials.

Material	Etch rate (Å/min)
Photoresist	300 to 500
Platinum	180
PZT	70
Silicon dioxide	50

Figure 6. Etched platinum electrodes.

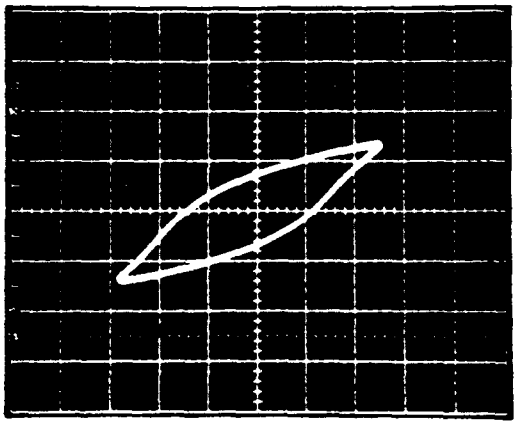


(a) 80 × 80 μm



Vertical: 5 mV/div
Horizontal: 2 V/div

(b) 40 × 40 μm



Vertical: 2 mV/div
Horizontal: 2 V/div

Figure 7. Hysteresis loops.

The next process steps involve the patterning and etching of the PZT film. To etch the PZT, we used a buffered HF etch consisting of seven parts of 40-percent ammonium fluoride solution to one part 48-percent HF. The sample was placed in a Teflon dish filled with the etching solution and mildly agitated during the total time in the solution. This agitation was necessary to constantly expose the PZT surface being etched to fresh etchant that had not become depleted by the etching process. The actual etching times depended upon the PZT film thickness, but an approximate etching rate of 700 Å/min was observed for the films used in our work. It was noticed that unlike the etching of silicon dioxide or other films usually encountered in integrated-circuit processing, the etching of the PZT left a film that gave the surface a dirty and uneven-looking appearance. This film was easily removed by a brief (10 to 20 s) dip in 5-percent nitric acid. The photoresist was then removed as before. Figure 8 shows the etched 40- × 40-μm PZT islands with the top platinum electrodes after the photoresist removal in the plasma asher as before. The capacitors were again characterized and found to be unchanged.

The final step in the fabrication process is the definition of the bottom electrode, by the same procedure used to etch the top platinum electrode. However, since the bottom platinum layers were somewhat thicker than the top, and because the titanium layer etches more slowly than the platinum, the time to sputter-etch the bottom electrode was increased to about 45 min. Figure 9 shows the etched bottom electrode plus the remaining photoresist. The photoresist was removed in the plasma asher as before, but this time we immersed the electrode for 5 min in Posistrip 830 maintained at a temperature of 105°C. Figure 10 shows a profile of the three-layer capacitor structure after photoresist removal. Despite the additional time required to etch the bottom electrode, the photoresist provided very good masking of the underlying capacitor structures. Figures 11 and 12 show a photomicrograph of one of the test cells and a photograph of the entire 4-in. wafer.

Figure 8. Etched PZT islands.

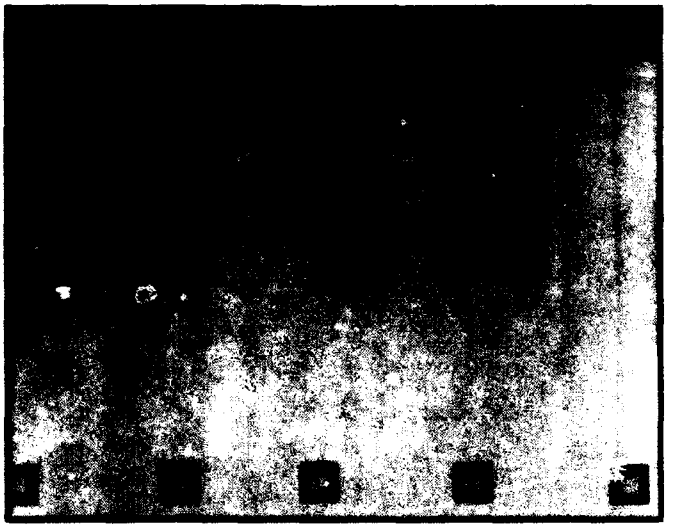


Figure 9. Etched bottom electrode.

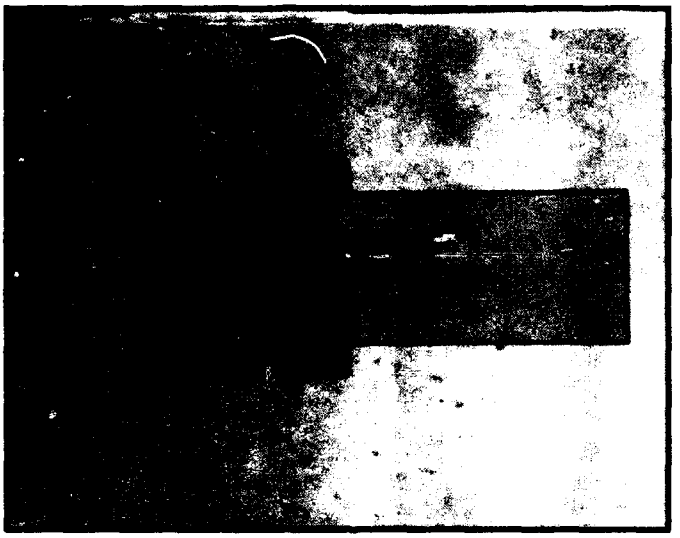


Figure 10. Topology of 80-μm ferroelectric capacitor.

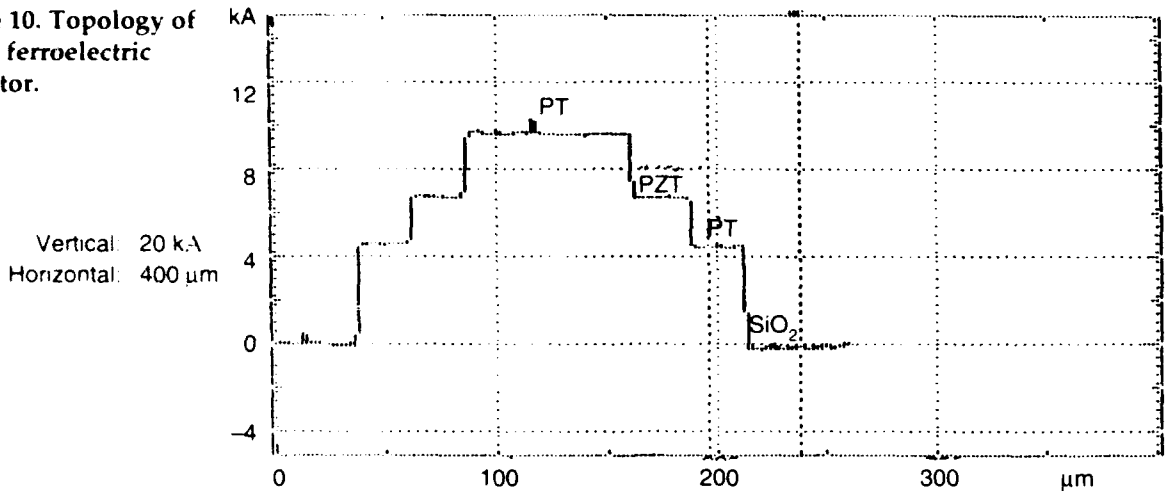


Figure 11. Photomicrograph of test cell.

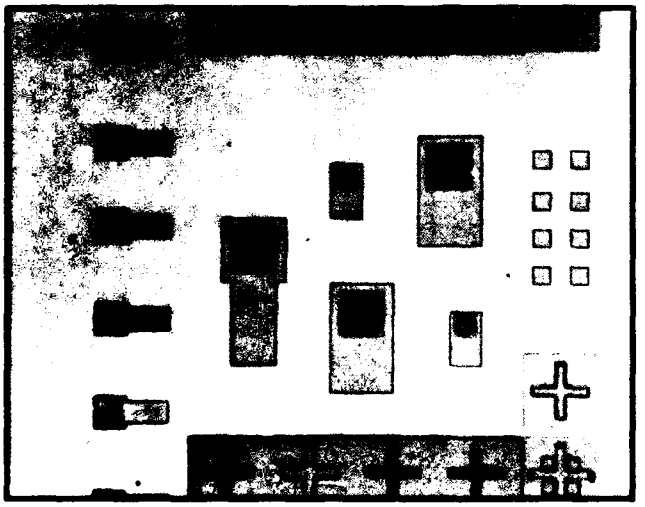
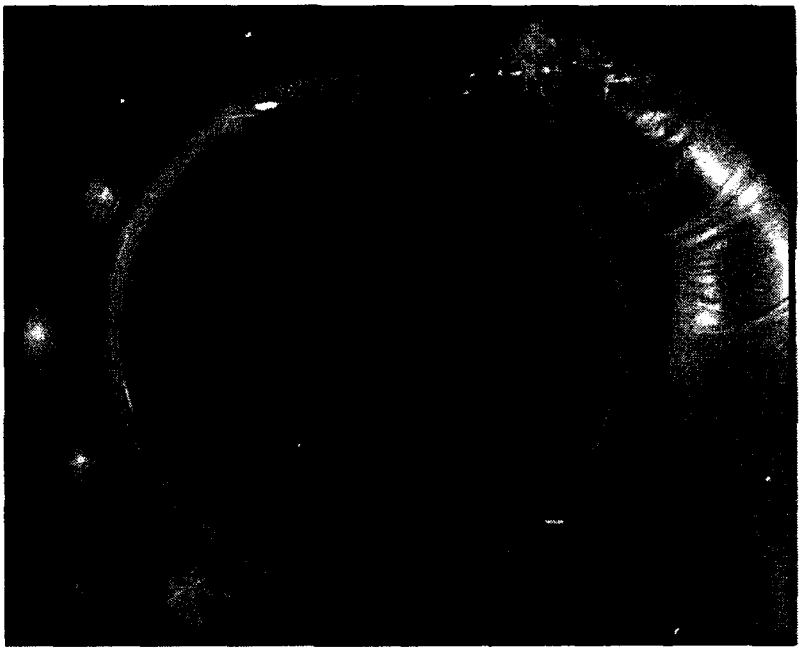


Figure 12. Completed wafer.



5. Device Test Results

We again point out that the ferroelectric films used in this work were not optimized to yield the best possible electrical characteristics. Nevertheless, it is worthwhile to consider the resulting electrical characteristics, if only to identify any possible degradation in the expected capacitor characteristics compared to previous measurements obtained on earlier films that saw no processing beyond shadow-mask-defined sputtered platinum electrodes. Figure 13 shows the hysteresis loops for the two different sizes of fully processed capacitors. Comparing these with the first hysteresis loops in figure 7 we see that no observable change has occurred in the devices as a result of the additional processing. A more precise analysis of the final electrical characteristics for the 80-μm device was obtained using an RT-66A ferroelectric tester. The results of these measurements are presented in figure 14. The total switched charge for the charge program hysteresis loop is observed to be 25 $\mu C/cm^2$, and the critical field about 69 kV with 5 V applied. Using the retained charge program, the 1-s retained switched charge for these devices was about 10 $\mu C/cm^2$. Details of the retained charge measurements are given in appendix A.

The measurement results presented here are similar to those obtained on earlier ferroelectric films that were prepared in the same way as the films discussed here, but with the top electrodes defined through a shadow mask so that no further processing was required to produce measurable capacitors.

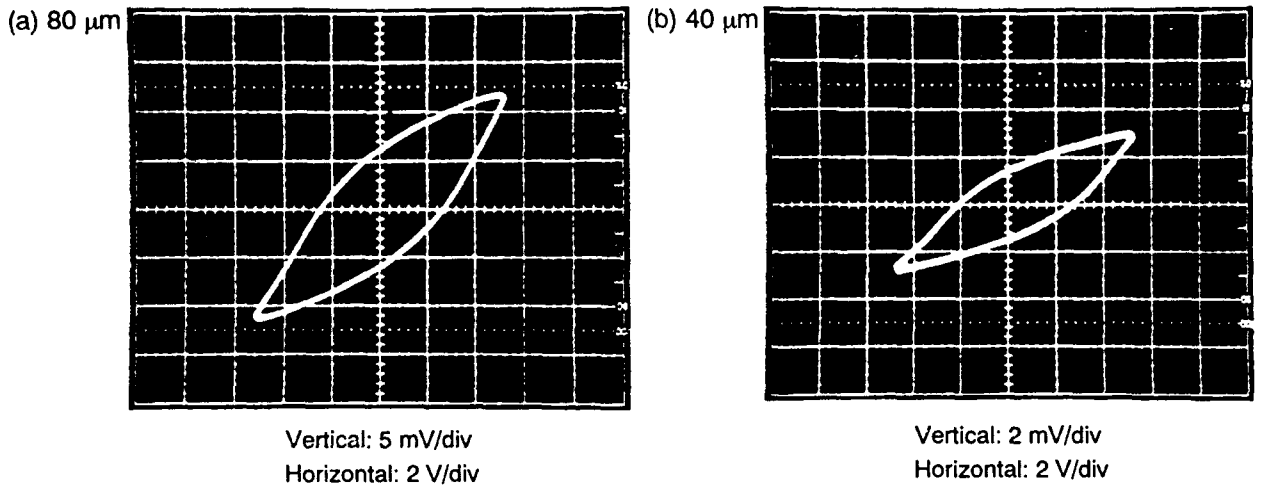
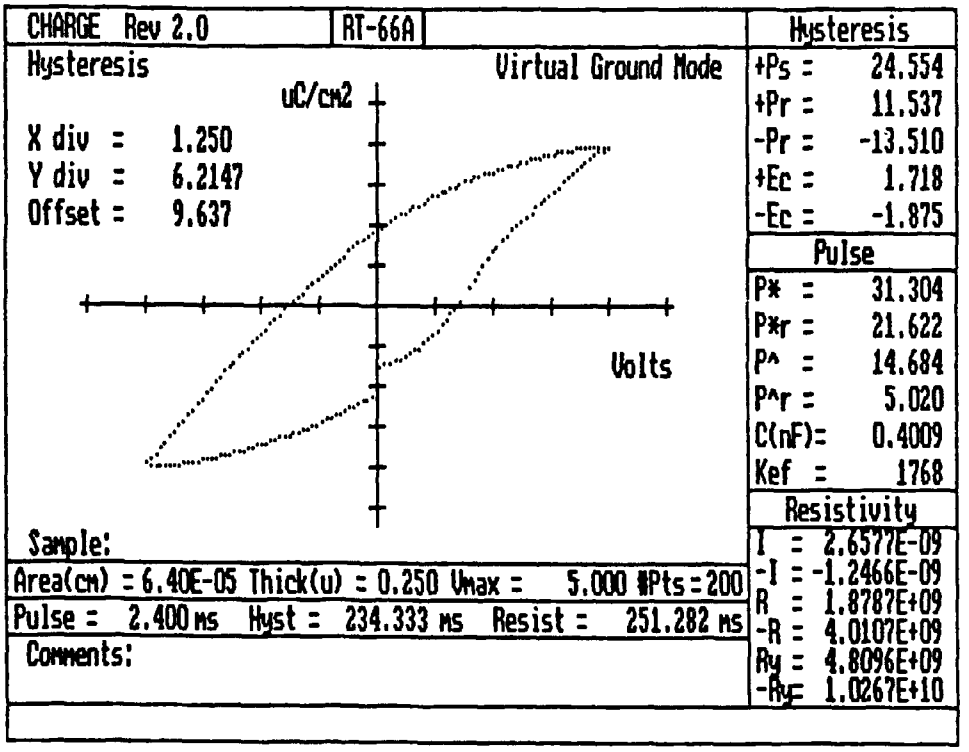


Figure 13. Hysteresis loops of fabricated capacitors.

Figure 14. RT66A results for 80-μm capacitors.



6. Conclusions

We have demonstrated a process for fabricating ferroelectric capacitors in a manner that is expected to be fully compatible with CMOS integrated circuits that have been processed up to, but not including, the first aluminum metal layers. The hysteresis characteristics for the fabricated ferroelectric capacitors remained essentially unchanged through the processing sequence, and were very similar to the characteristics of capacitors produced on unprocessed ferroelectric films with the top electrodes defined by a shadow mask. The integration of the fabricated capacitors into an existing CMOS circuit would consist of preparing the CMOS wafer for the bottom platinum electrode deposition, passivating the completed capacitors using a deposited oxide or other suitable film, opening contact windows, and depositing and defining the metal layers. Work is currently in progress to define suitable passivation and metalization techniques, and to demonstrate a fully functional CMOS/ferroelectric capacitor memory element produced by the process described here.

Acknowledgments

The author wishes to gratefully acknowledge the assistance of the following persons during the work discussed herein: J. McCullen for the pattern imaging, J. Terrell of Booz, Allen, and Hamilton, Inc., for most of the platinum sputtering and sputter etching, and R. Moore for the RT66 test results.

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Appendix A.—Retained Charge Measurements

```
Acquisition Program Name:  RETAIN  2.0

Data File Name:     No Valid File

    Sample:
    Date of Test:

    Sample Area:  0.00006 cm
    Sample Thickness:  0.250 μm

    Vwrite:    5.000  volts          Vscale:    1.000
    Vread:     5.000  volts
    DCBias:      0.00  volts        Contacts:  CLOSED
    Type Data: RETAINED SIGNAL   in Virtual Ground Mode

    Csense:   0.00470 μF    Iscale: 1.000      Ext. Iscale:  1.000
    Capacitor Measurement  Amplification:  10.00000

    Number of Retention Periods:   5
    Write Pulse Width = 0.0086 milliseconds
    Read Pulse Width =  2.300 milliseconds

COMMENTS:

 RESULTS:

     Profile #5
       P*  =    15.276 μC/cm2
       P*r =     5.881 μC/cm2
      -P*  =  -21.622 μC/cm2
      -P*r =  -15.276 μC/cm2

 PROFILE:

   Retention Period# 1 =  0.30 seconds
   Retention Period# 2 =  1.00 seconds
   Retention Period# 3 =  3.00 seconds
   Retention Period# 4 = 10.00 seconds
   Retention Period# 5 = 30.00 seconds
```

Appendix A

RETAINED SIGNAL of Sample: for a 0.0086 ms Vwrite WRITE pulse and a 2.300ms Vread READ pulse with a 0.00 volts bias with contacts CLOSED after the following RETENTION periods:

Retention Period# 1 = 0.30 seconds.

+P* [1]	=	15.383 μC/cm2
+P*r[1]	=	5.863 μC/cm2
−P* [1]	=	−22.788 μC/cm2
−P*r[1]	=	−16.029 μC/cm2

Retention Period# 2 = 1.00 seconds.

+P* [2]	=	15.096 μC/cm2
+P*r[2]	=	5.594 μC/cm2
−P* [2]	=	−22.626 μC/cm2
−P*r[2]	=	−15.921 μC/cm2

Retention Period# 3 = 3.00 seconds.

+P* [3]	=	15.150 μC/cm2
+P*r[3]	=	5.684 μC/cm2
−P* [3]	=	−22.411 μC/cm2
−P*r[3]	=	−15.742 μC/cm2

Retention Period# 4 = 10.00 seconds.

+P* [4]	=	15.258 μC/cm2
+P*r[4]	=	5.773 μC/cm2
−P* [4]	=	−22.071 μC/cm2
−P*r[4]	=	−15.598 μC/cm2

Retention Period# 5 = 30.00 seconds.

+P* [5]	=	15.276 μC/cm2
+P*r[5]	=	5.881 μC/cm2
−P* [5]	=	−21.622 μC/cm2
−P*r[5]	=	−15.276 μC/cm2

```
Acquisition Program Name: RETAIN   2.0

Data File Name:     No Valid File

    Sample:
    Date of Test:

    Sample Area:  0.00006 cm
    Sample Thickness:  0.250 µm

    Vwrite:    -5.000  volts        Vscale:    1.000
    Vread:      5.000  volts
    DCBias:       0.00  volts      Contacts:  CLOSED
    Type Data: RETAINED SIGNAL   in Virtual Ground Mode

    Csense:   0.00470 µF    Iscale: 1.000      Ext. Iscale:  1.000
    Capacitor Measurement  Amplification:  10.00000

    Number of Retention Periods:   5
    Write Pulse Width = 0.0086 milliseconds
    Read Pulse Width =  2.300 milliseconds

COMMENTS:

 RESULTS:

     Profile #5
       P*  =    23.631 µC/cm2
       P*r =    13.841 µC/cm2
      -P*  =   -21.461 µC/cm2
      -P*r =   -14.128 µC/cm2

 PROFILE:

   Retention Period# 1 =  0.40 seconds
   Retention Period# 2 =  1.00 seconds
   Retention Period# 3 =  3.00 seconds
   Retention Period# 4 = 10.00 seconds
   Retention Period# 5 = 30.00 seconds
```

Appendix A

RETAINED SIGNAL of Sample: for a 0.0086 ms Vwrite WRITE pulse and a 2.300ms Vread READ pulse with a 0.00 volts bias with contacts CLOSED after the following RETENTION periods:

Retention Period# 1 = 0.40 seconds.

+P* [1]	=	26.302 μC/cm2
+P*r[1]	=	16.459 μC/cm2
−P* [1]	=	−21.891 μC/cm2
−P*r[1]	=	−14.361 μC/cm2

Retention Period# 2 = 1.00 seconds.

+P* [2]	=	24.921 μC/cm2
+P*r[2]	=	15.096 μC/cm2
−P* [2]	=	−21.909 μC/cm2
−P*r[2]	=	−14.379 μC/cm2

Retention Period# 3 = 3.00 seconds.

+P* [3]	=	24.455 μC/cm2
+P*r[3]	=	14.684 μC/cm2
−P* [3]	=	−21.909 μC/cm2
−P*r[3]	=	−14.343 μC/cm2

Retention Period# 4 = 10.00 seconds.

+P* [4]	=	24.097 μC/cm2
+P*r[4]	=	14.236 μC/cm2
−P* [4]	=	−21.730 μC/cm2
−P*r[4]	=	−14.289 μC/cm2

Retention Period# 5 = 30.00 seconds.

+P* [5]	=	23.631 μC/cm2
+P*r[5]	=	13.841 μC/cm2
−P* [5]	=	−21.461 μC/cm2
−P*r[5]	=	−14.128 μC/cm2

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